WSI Implemented with Button Board Interconnection

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ABSTRACT

Development of a cheap, high yield interconnection technology is crucial to implementing WSI circuits. However, limitations in process yield and the design complexity experienced with monolithic (on-wafer) interconnect have prevented WSI from being commercially feasible. Button contacts, by providing a means of interconnecting working die for WSI processors external to the wafer, fulfill the requirements of WSI at significantly lower cost than monolithic approaches. After probe test, a printed circuit board is combined with button contacts to provide a flexible method of achieving the discretionary interconnect to good die. A prototype package has been built which demonstrates the feasibility of our WSI interconnect and packaging approach. We will discuss the button board packaging approach, the electrical characteristics of our button contact interconnect along with future applications of this technology.

Introduction

TRW is pursuing multiple development paths towards Wafer Scale Integration (WSI). The approach described in this paper uses a button board discretionary wafer interconnect to produce a "semi-monolithic" approach. It complements the rather widely publicized superchip approach, the CPUAX, that implements monolithic wafer interconnect.

WSI Interconnect

The occurrence of defects during fabrication forces a dichotomy in WSI design between the physical layout of the wafer (a map of functional and defective cells), and the virtual layout of the wafer (a map of the desired cells). Coercing agreement between the physical and virtual layouts is the role of the interconnect. With monolithic designs, the interconnect is placed on the wafer as an integral part of the functional architecture. Sufficient redundancy of interconnect paths and components must be provided to work around defective circuitry. In the case of monolithic discretionary interconnect, wafer sites are probe tested and then functional parts are 'hooked up' as a final fabrication step.

Our approach is similar in many respects to that of MIT Lincoln Labs. Wyatt and Raffel[1] have reported on discretionary wiring using a test and configure approach to eliminate routing channels. After the wafers are probe tested one cell at a time, a laser is used to burn away connections to faulty cells as well as make connections to good cells using a proprietary 'antifuse' technology. The test and anti-fuse steps are repeated one cell at a time, until the process of linking all of the desired cells to form the WSI circuit is complete. The Lincoln Labs approach requires some forethought during the design phase to facilitate the circuit routing and redundancy requirements. In addition, the

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process steps required for implementing the circuit interconnection can introduce additional wafer defects.

Our button board packaging approach replaces the Lincoln Labs "cut and join" technique with a discretionary interconnect that is external to the wafer. The button board interconnect is applied after the wafer is fabricated and probe tested, and requires no additional process steps. In addition, for optimal yields, the interconnect may be modified to implement virtual layouts other than the initial configuration. This approach uses conventional cell designs and wafer fabrication techniques which reduce development cost and allows increased design and process flexibility. The designer is, therefore, free to use any cell design or process in implementing a WSI device, and can quickly modify the interconnection to adapt to changes in the circuit architecture.

Button Board Interconnect

The conventional button board interconnect is a TRW-developed technique of interconnecting circuit boards using button contacts, small diameter (<40MIL) cylinders of gold-plated copper wire. Boards are connected using the button contacts by fabricating pad areas on the back sides of the boards (not component side). The boards are then stacked with mating pad areas facing each other. Between the boards is placed a dielectric spacer board, with holes drilled at locations corresponding to the mating pad areas. These holes are filled with conductive buttons which make the connection between mating pad areas. A button is placed within the hole to make a connection, or omitted to disconnect a pad.

For WSI the button board simplifies the problems associated with interconnect by allowing connections to be made across the entire wafer surface. As shown in figure 1, a button board is fabricated with button contacts installed at locations corresponding to the pads of each cell on the wafer. The button board is placed over the wafer, with button contacts inserted in the holes.

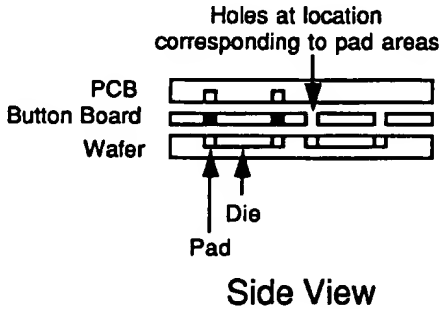

Figure 1. Button Board Interconnect

An interconnect printed circuit board (PCB) with pad areas matching the button contact locations is placed over the button board (pads facing the button board). Interconnect between functional sites on the wafer is made by PCB traces. Shown in Figure 2., the three layer assembly: wafer, button board and interconnect PCB, is placed within a

surface mount leaded package. Interconnect from the wafer to the package I/O pads (leads) is also made via the button contact and interconnect PCB. The wafer is precisely sawed to fit and align within the package cavity. The wafer thickness is also controlled so that its surface is coplanar with the package I/O pad surface. The button board and interconnect PCB are designed larger than the wafer (cavity) and overlap the package I/O pad area. Connection between the interconnect PCB and the package leads is made in the overlap area using additional button contacts. The button board and interconnect PCB both align to the package seal ring for button to pad alignment. The package lid applies sufficient pressure to the assembly to ensure contact between the three layers.

Current technological limitations in button contact size (diameter) place constraints on the pad size of wafer sites. In current manufacturing practice, devices are designed with 5 mil pads on 8 mil centers. Use of button boards requires larger pads to remain compatible with button insertion techniques. The larger pads allow for movement during assembly and for dimensional variations caused by heat or shock during device operation. Figure 3. shows a wafer with potential cell sites. Figure 4. shows a site modified for use with button interconnect. The original pad ring with 5 mil pads is shown inside the new pad ring.

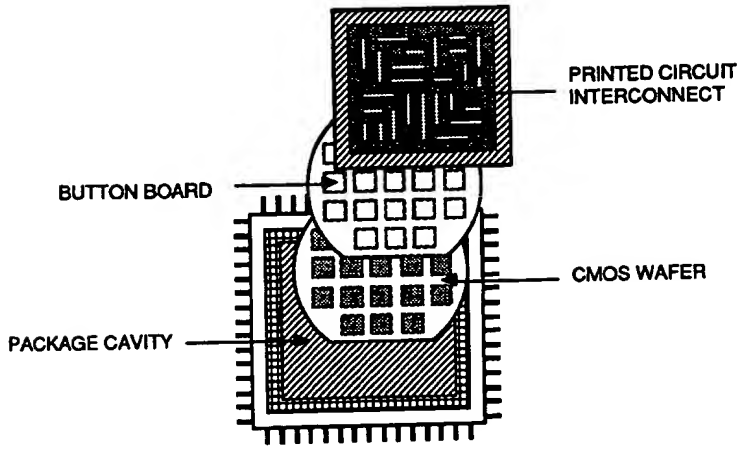

Figure 2. Packaged Button Board Interconnect

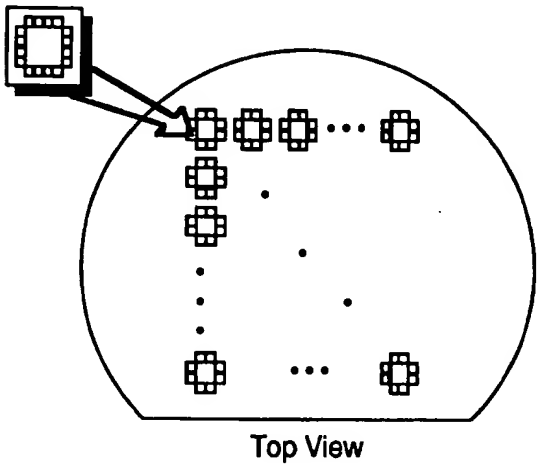

Figure 3. Wafer With Potential Cell Sites

Retaining the original pad ring allows a conventional probe card to be used in testing. The redesign required for the expanded pad-ring requires additional space on the wafer, reducing the overall yield. However, the benefits of reduced routing constraints, lower development cost, and increased flexibility help off-set the reduction in available die area.

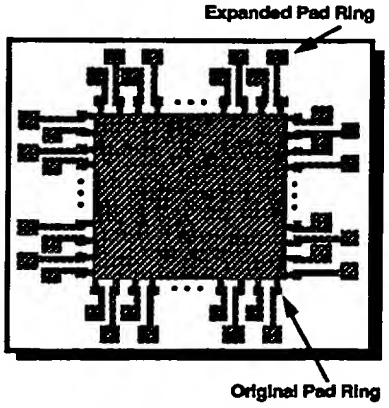

Figure 4. Modified Cell Site With Expanded Pad Area

For experimental purposes, the modified pad ring with larger pads and pad spacing may be designed into the final metal layer or,may be applied using E beam lithography. Whereas redesigning the mask is preferable for production quantities, using the E beam

or experimental purposes, the modified pad ring with larger pads and pad spacing may be designed into the final metal layer or,may be applied using E beam lithography.

Current Work

For this work, a prototype wafer was fabricated implementing a passive interconnect only. In our preliminary development, this approach allows better characterization of the button interconnect electrical characteristics than would an array of active devices. To speed the next stage of development, a cell inner pad ring identical to that of a candidate processor, the LSI Products TMC3202 (floating point multiplier/adder) was used. E beam processing was used to write both the inner (existing) pad ring and the larger (modified) pad ring required for the button interconnect. A trace pattern such as that shown in Figure 2. was used to interconnect pads. A single area corresponding to a 4 X 4 grid of cells was diced from the four inch wafer and assembled into the package.

The printed circuit board was designed to interconnect several of the cells on the wafer to provide data on button contacts and traces interconnected across the whole wafer and across multiple cells. After assembly of the three layer system (wafer, button board, PC interconnect board) into the package, the integrity of the button contact interconnect may be evaluated. Preliminary results indicate a button capacitance of less than 2pF or one fifth the lead capacitance of conventional VLSI packaging.

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[1] Peter W. Wyatt, and Jack I. Raffel, "Restructurable VLSI - A Demonstrated Wafer Scale Technology", International Conference On Wafer Scale Integration, San Francisco, CA 3-5 January 1989.